MER HOME I SEARCH HERE I SHOP I WEE ACCOUNT I CONTACT HERE Publications/Services Standards Conferences Careers/Jobs IEEE Xpiore® Welcome 1 Million Developers 1 Million Users **United States Patent and Trademark** Office » Search Results FAQ Terms IEEE Peer **Quick Links** Review Your search matched 5 of 1099265 documents. C>- Horme A maximum of 500 results are displayed, 15 to a page, sorted by Relevance O- Wited Can in **Descending** order. Access? C- Lon-out **Refine This Search:** tables of Contents You may refine your search by editing the current search expression or entering a new one in the text box. ()- Journals reconfigurable <and> accumulation <and> addition Search 8: Magazines 🗘 Conterence Theck to search within this result set Proceedings O- Standards **Results Key: JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard Search O- By Author 1 Accelerating pipelined integer and floating-point accumulations in C> Basin configurable hardware with delayed addition techniques O- Advanced Luo, Z.; Martonosi, M.; ( )- CrossRef Computers, IEEE Transactions on , Volume: 49 , Issue: 3 , March 2000 Pages: 208 - 218 O: 3000 1888 [Abstract] [PDF Full-Text (2492 KB)] IEEE JNL O- Establish IEEE West Account 2 Using learning techniques to accommodate unanticipated faults Cr Access the Farrell, J.; Berger, T.; Appleby, B.D.; IEEE Member Control Systems Magazine, IEEE , Volume: 13 , Issue: 3 , June 1993 Digital Library Pages:40 - 49 [Abstract] [PDF Full-Text (972 KB)] IEEE JNL O- 6000000 1100 VEEK Endominisie File Cobost 3 Image processing chip for small object detection LeRiguer, E.; Woods, R.; Ridge, D.; McCanny, J.; Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G-Print Format Circuits, Devices and Systems], Volume: 146, Issue: 2, April 1999 Pages:49 - 54 [Abstract] [PDF Full-Text (604 KB)] IEE JNL 4 A sub-word parallel digital signal processor for wireless communication systems Yuan-Hao Huang; Tzi-Dar Chiueh; ASIC, 2002. Proceedings. 2002 IEEE Asia-Pacific Conference on , 6-8 Aug. 2002 Pages: 287 - 290 [Abstract] [PDF Full-Text (319 KB)] IEEE CNF 5 Efficient implementation for high accuracy DCT processor based on

FPGA
Naviner, L.: Danger, J.-L.: Laurent, C.: Garcia-Garcia, A.:

Naviner, L.; Danger, J.-L.; Laurent, C.; Garcia-Garcia, A.; Circuits and Systems, 1999. 42nd Midwest Symposium on , Volume: 1 , 8-11 Aug. 1999

Pages:508 - 511 vol. 1

[Abstract] [PDF Full-Text (372 KB)] IEEE CNF

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this